
Functions

Digital Trunk Interface

The QPC472/QPC720 Digital Trunk Interface (DTI) card is the interface between any selected channel of the 32-channel, 2.048 Mbps bit stream on the associated Meridian 1 Network loop and a DS-1, 24-channel, 1.544 Mbps, bipolar carrier terminal.

DTI software

The DTI software module performs the following procedures in supporting the DTI feature:

- processes messages from the DTI hardware
- handles transmission loss pad settings
- handles Echo Canceller control
- processes online performance monitoring functions of the DTI
- inserts and translates call types (voice or data)
- converts a DTI Terminal Number (TN) to an equivalent loop and channel or a loop and channel to an equivalent TN
- periodically checks the Clock Controller (CC)
- switches the reference clock from primary to secondary source if unable to track on primary
- switches the reference clock from secondary to free run if unable to track on secondary
- updates the tracking of the Clock Controller after a change of primary or secondary reference source, or after sysload

Meridian 1/DS-1 conversion

Flexible mapping of 30 network time slots into 24 DS-1 channels (conversion from bit-interleaved to byte-interleaved format) and vice versa is performed by the DTI.

Idle, unequipped, or disabled DS-1 channel states

For each DS-1 channel that is idle or not configured, DTI hardware transmits “idle” (7F hexadecimal) or “unassigned” (FF hexadecimal) Pulse Code Modulation (PCM) codes respectively during the voice/data time slots. The DTI hardware and software data blocks are initialized to the appropriate idle or disabled state after system configuration, or following service change, and after every initialization. Other DS-1 systems receiving these signals interpret them as idle and unassigned, respectively.

Processing of A & B signaling bits

The DTI software sets the transmitted A & B bits to represent the appropriate signals for the trunk being supported. It also interprets the received A & B bit states as appropriate signaling states for that trunk.

Control of pad switching

The DTI inserts digital pads for both transmit and receive directions on a per channel basis, to achieve the desirable port-to-port transmission loss values. DTI channels are classmarked for different trunk types for pad-setting and signaling purposes.

Meridian 1 data protocol converter

The Meridian 1 data protocol, which uses 8 bits for data, is not compatible with DS-1 protocol. Transmission on DS-1 facilities requires a “ones” density not compatible with data. Also, if A & B bits are processed on the link, the least significant bit of the 8-bit Pulse Code Modulation (PCM) word in the signaling frames is used for A & B signaling. For this reason, protocol conversion is provided to originating and terminating data messages on a per call basis at the originating and terminating DTIs. After trunk, line, and address signaling is complete and a path has been established between the two data terminals, the protocol converter is switched in until the call is disconnected.

Echo Canceller control

Echo Cancellers are required for satellite applications only. The DTI software controls external Echo Cancellers on a per channel basis by means of an RS232-C link. The Echo Canceller usually remains enabled. For data calls however, the DTI hardware disables the Echo Canceller. When the Meridian 1 is connected to another switching node equipped with Echo Cancellers that do not provide per call control, specific time slots can be permanently marked as data only.

Maintenance functions

The DTI performs maintenance functions related to the DS-1/D3 format link, including monitoring and reporting. It also does a self-check.

Data transmission and reception

DTI transmits and receives bipolar return-to-zero data at DS-1/D3 signal levels. Zero code suppression is normally in effect but may be inhibited as required by DTI software.

Controlled slips

DTI deletes or repeats frames of information from time to time in the receive Pulse Code Modulation (PCM) direction to allow for signals that may be running at a slightly different bit rate to the DTI (that is, controlled by the transmitting system clock).

Clock Controller synchronization

Digital communication requires accurate timing alignment of digital signals so that data is interleaved into or extracted from the appropriate timeslots during multiplexing and demultiplexing operations. Frame synchronization can be attained by having all switches and transmission facilities in a network controlled by clocks of the same frequency. This is achieved by having all nodes (switches) in a network locked to a primary frequency source (a master clock).

Synchronization criteria

North American digital network nodes are synchronized using a priority master-slave method. Digital nodes are ranked in categories (AT&T Strata 1 to 4 or Bell Canada Node Category A to E). Each node is synchronized to the highest ranking node in its vicinity with which it has a direct digital link.

The Clock Controller (CC) meets AT&T Stratum 3 and Bell Canada Node Category D synchronization criteria. The clock has a drift rate of less than one part in 10^9 per day when the clock is in free running mode.

Clock Control

The clock synchronization subsystem for DTI is provided by a single card on single CPU systems or a duplicated pair of Clock Controller (CC) cards on dual CPU systems. On dual CPU systems, only one CC is active at any given time. The disabled clock serves as a standby to the first.

When the clock subsystem is synchronized to an external clock source through a specific DTI defined as a reference clock source, it is said to run in Tracking Mode. When no reference source is defined, or when the clock subsystem is not locked onto the external clock source, it is in Non-Tracking Mode and running free. In this case, there is no synchronization between the Meridian 1 and the external network. Where more than one DTI loop exists, primary and secondary reference clock sources can be defined for Tracking Mode operation.

The active CC in the subsystem performs the following functions:

- synchronizes to a primary or secondary reference clock (in Tracking Mode)
- supplies Meridian 1 with a clock

Tracking supervision

Meridian 1 software periodically (every 15 minutes) monitors the Clock Controller (CC) status. If the CC is unable to track the reference source, Meridian 1 sends a message to the system terminal. If automatic switching is defined in the CC data block, the Meridian 1 switches as follows:

Unable to track on	Switch CC to
Primary	Secondary
Secondary	Free-run

Meridian 1 performs the same operation if a DTI that is a primary or secondary reference clock source is placed out of service.

Bit error rates

Bit error rate monitoring detects errors in transmission. There are two methods of bit error rate monitoring, bipolar violation (BPV) tracking and cyclic redundancy check (CRC). The method used depends on the framing format (D2, D3, D4, or Extended Superframe [ESF]). Framing format is defined in LD17 prompt DLOP.

Bipolar violation (BPV) In a bipolar pulse stream, pulses alternate in polarity. If, after transmission, two pulses of the same polarity are received in succession (this could be caused by an electrical disturbance, such as noise), a bipolar violation has occurred.

Cyclic redundancy check (CRC) The primary difference between Bipolar Violations (BPV) and CRC is that BPVs indicate errors on the local span, while CRC indicates errors on an end-to-end span. For example, on a satellite link, BPV only detects errors in the span between the Meridian 1 and the satellite connection. Since CRC travels between the entire span, it indicates end-to-end bit error rate. In DTI with ESF, bit error rate checking is done as CRC; however, the BPV counter is incremented.

Frame slip

Digital signals must have accurate clock synchronization for data to be entered into or taken from the appropriate timeslot during multiplexing and demultiplexing operations. Frame slip monitoring detects frame deletion and repetition errors in clock synchronization.

Frame alignment

Loss of frame alignment monitoring detects out-of-frame conditions on the DS-1 bit stream.

Loss of frame alignment thresholds DTI hardware detects out-of-frame conditions. The midnight routines print the number of loss of frame alignment occurrences and clear the counters.

There are three frame alignment thresholds set in LD73. When a maintenance or out of service threshold is reached, a data terminal allowed (DTA) message is output:

- DTA019: Frame alignment maintenance limit.
- DTA020: Frame alignment out of service limit.

If a loss of frame alignment condition persists for three seconds, the affected DTI loop is taken out of service and a red alarm is raised. If the loss of frame alignment condition clears for at least 15 seconds, the DTI is automatically restored to service. The following data terminal allowed (DTA) message is generated:

- DTA021: Loss of frame alignment has persisted for 3 seconds.

Clock distribution

Multi-group mode (XN and XT) Each Clock Controller (CC) continuously drives the following signals to the IGS cards:

- M8 (8 MHz system clock)
- MFS (4 kHz sync pulse)
- CLKEN (clock enable active/disabled)

Single- or half-group mode (N, NT, and RT) Each CC continuously drives the following signals to PS cards:

- M8XB (8 MHz system clock)
- MFSB (4 kHz sync pulse)

Half-group mode (MS, ST) The optional single CC operates in the half-group mode and supplies the clock. Should the clock fail, there is no switchover, and the PS card provides the clock.

Clock switchover

Each of the two CC cards monitors the other for clock failure and responds to switchover requests from its twin or from the CPU.

Phase locked loop

CC synchronization is achieved by phase locking to a 4 kHz clock derived from the 1.544 MHz reference source selected by the CPU. If the reference clock is lost, the CCs run free.

Automatic clock recovery

An option for automatic clock recovery can be selected in LD60 with the command EREF.

A DTI loop is disabled when it enters a red alarm (local) condition. If the red alarm is cleared, the loop is enabled automatically. When the loop is enabled, clock tracking is restored with the following conditions:

- If the loop is assigned as the primary reference clock but the CC is tracking on the secondary reference or in free run mode, it is restored to tracking on primary.
- If the loop is assigned as the secondary reference clock but the CC is in free run mode, it is restored to tracking on secondary.

If the 15-minute clock check indicates the system is in free run mode:

- Tracking is restored to the primary reference clock if defined.
- If the primary reference is disabled or in red alarm, (local) tracking is restored to the secondary reference clock if defined.

If the EREF option is selected in LD60, tracking on the primary or secondary reference clock is automatically switched in the following manner:

- If software is unable to track on the assigned primary reference clock, it switches to the secondary reference clock and sends appropriate DTC maintenance messages.
- If software is unable to track on the assigned secondary reference clock, it switches to free run.